REMARKS

This is intended as a full and complete response to the Office Action dated October 16, 2008, having a shortened statutory period for response set to expire on January 16, 2009. Please reconsider the claims pending in the application for reasons discussed below.

In the specification, paragraph [0014] has been amended to correct minor editorial problems.

Claims 1-16, 18-27 and 34 are pending in the application. Claims 1-10, 12-14, 16, 18-27, 34, 36, and 37 remain pending following entry of this response. Claims 1, 14, 16, 18, 26, and 34 have been amended. Claims 11 and 15 have been cancelled. New claims 36 and 37 have been added to recite aspects of the invention. Applicants submit that the amendments and new claims do not introduce new matter.

Further, Applicants are not conceding in this application that those amended (or canceled) claims are not patentable over the art cited by the Examiner, as the present claim amendments and cancellations are only for facilitating expeditious prosecution of the claimed subject matter. Applicants respectfully reserve the right to pursue these (pre-amended or canceled claims) and other claims in one or more continuations and/or divisional patent applications.

Claim Rejections - 35 U.S.C. § 103

Claims 1, 16, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Owen et al.*, U.S. Patent No. 5,161,157 (hereinafter *Owen*) in view of Applicant's admitted prior art.

Claims 1- 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Oonk*, U.S. Patent No. 6,862,703 in view of *Deas*, U.S. Patent No. 6,065,090.

Claims 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Oonk* in view of Applicant's admitted prior art.

Claims 16, 18-21, 23-25, 27, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Schwartz*, U.S. Patent No. 6,795,942 in view of *Deas*.

Claims 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Schwartz*.

The Examiner bears the initial burden of establishing a prima facie case of obviousness. See MPEP § 2141. Establishing a prima facie case of obviousness begins with first resolving the factual inquiries of Graham v. John Deere Co. 383 U.S. 1 (1966). The factual inquiries are as follows:

(A) determining the scope and content of the prior art;

(B) ascertaining the differences between the claimed invention and the prior art;

(C) resolving the level of ordinary skill in the art; and

(D) considering any objective indicia of nonobviousness.

Once the Graham factual inquiries are resolved, the Examiner must determine whether the claimed invention would have been obvious to one of ordinary skill in the art.

Regarding claims 1 and 16, as amended herein, and the claims depending therefrom, the cited references do not disclose overwriting stored addresses of one of columns and rows having a first number of defective storage cells with addresses of one of columns and rows having a second number of defective storage cells, wherein the second number is greater than first number. Examiner suggests that this claim element is disclosed in Column 2: Lines 5-26 of *Oonk*, provided below.

> The test apparatus includes an error capture memory for keeping track of the defective cells, but also includes a separate counter for each row and each column of the array. Whenever the tester finds a defective memory cell, it not only makes note of the failed cell in the error capture memory, it increments the count of the counters corresponding to the defective cell's row and column. Thus at the end of a memory test, the counts indicate the number of defective cells in each row and in each column. The tester sends the counts to a computer which can usually determine how to allocate spare rows and columns to repair the memory on the basis of the counts alone. The test apparatus therefore sends data from the error capture memory to the computer only when the computer is unable to determine how to repair the memory solely on the basis of counts. The system is advantageous because the test apparatus can forward the relatively small amount of count data to the computer much faster than the relatively large amount of error capture memory data. However since the test apparatus must provide a separate counter for each row and column of the array, the apparatus requires a large number of counters in order to test memories having a large number of rows and columns. *Oonk*, Column 2: Lines 5-26.

Applicants respectfully submit that the cited lines above only discloses providing separate counters for counting defective cells in each row and column of memory. There is nothing in the above lines, however, regarding overwriting stored addresses of one of columns and rows having a first number of defective storage cells with addresses of one of columns and rows having a second number of defective storage cells.

Furthermore, regarding claim 34 and the claims depending therefrom, the cited references do not disclose a plurality of memory built-in self repair circuits, each memory built-in self repair circuit being associated to one of the plurality of memories and being configured to allocate at least one of redundant row elements and column elements for replacing respective one of rows and columns of the associated memory having defective storage cells, and at least one block of redundant word elements for replacing words containing defective storage cells without replacing the entire rows containing the words being replaced, wherein one block of redundant word elements is used for replacing words containing defective storage cells of the plurality of memories, and wherein replacing of the at least one word with a redundant word is accomplished after replacement of all rows or columns with redundant rows or columns. More specifically, neither *Owen* or *Schwartz* disclose a block of redundant words, wherein the block of redundant words is used for replacing defective memory cells in a plurality of memories, and wherein each of the plurality of memories is associated with a memory built-in self repair circuit configured to allocate at least one of redundant row elements and column elements for replacing respective one of rows and columns of the associated memory having defective storage cells.

Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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